Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 7. (Canceled).

8. (New) A method of simultaneously operating a sequential processor and a reconfigurable array, comprising:

transferring data from a data cache into a reconfigurable array; and

writing results produced from the data and in the reconfigurable array to a destination.

9. (New) The method according to claim 8, wherein said destination is upstream of an arithmetic logic unit of the sequential processor.

10. (New) The method according to claim 9, wherein data output from the reconfigurable array is, at least in part, fed into a data path of the sequential processor downstream of decoding circuitry of the sequential processor.

11. (New) The method according to claim 9, wherein the arithmetic logic unit of the sequential processor is adapted to perform at least one operation on data output from the reconfigurable array.

12. (New) The method according to claim 11, wherein at least one of:

the arithmetic logic unit includes circuitry for at least one of multiplication and division; and

the at least one operation includes at least one of multiplication, division, and norming.

13. (New) The method according to claim 8, wherein data output from the reconfigurable array is selectably writable to a memory location other than any of the cache and a register of the sequential processor.

14. (New) The method according to claim 8, wherein the destination is at least one of downstream of an arithmetic logic unit and upstream of the cache.

15. (New) The method according to claim 14, wherein the cache is coupled to the sequential processor.